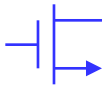
Advanced Analog Integrated Circuits

Part II

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu



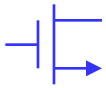
Implementation Issues

- Biasing
- Layout
- Interference
- Practical OTA architectures
- MOS Switches
- Matching, Offset
- Precision Techniques

Advanced Analog Integrated Circuits

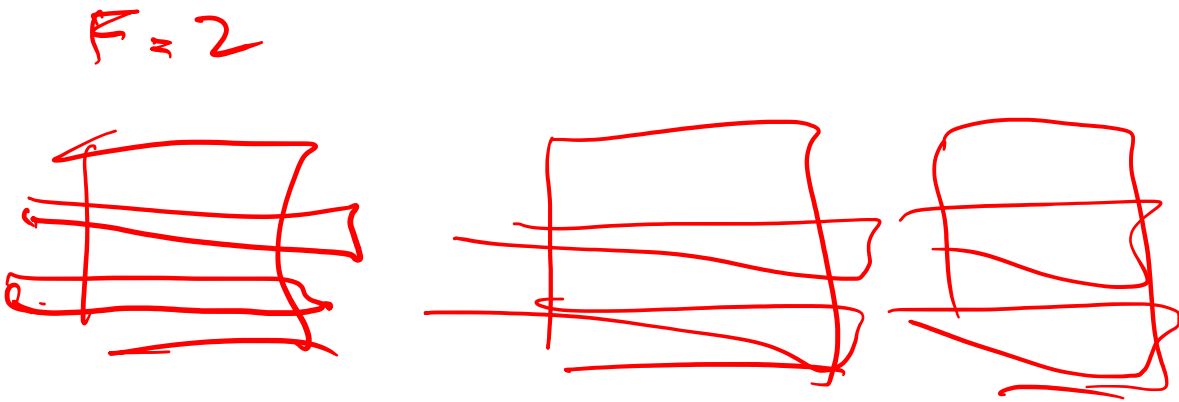
Biasing

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu



Transistor Biasing

- Design Parameter
  - $g_m,\ V^*,\ f_T$
- Layout Parameter
  - $W,\ L$
  - Fingers F
  - Multiplicity M



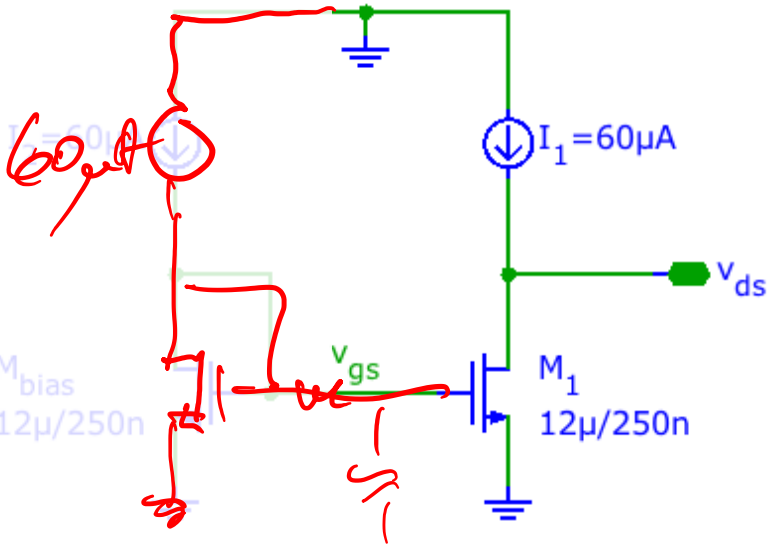
Example

Design: $g_m := 1mS$ $V_{star} := 120mV$ $f_T := 6GHz$

Layout (lookup): $L := 250nm$ $I_{d\_w} := 5\frac{A}{m}$

$$I_D := 0.5 \cdot g_m \cdot V_{star} = 60\,\mu A$$

$$W := \frac{I_D}{I_{d\_w}} = 12\,\mu m$$



CMOS 180
grade=nominal

OP Analysis OP1

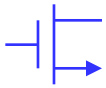
Spectre Syntax:

```
op1 dc oppoint=screen
```

Operating Point Analysis

```
 Instance: M1 of nmos3
    Model: nfet.4
Primitive: bsim3v3
        d : V(v_ds) = 523.447 mV
        g : V(v_gs) = 523.447 mV
        s : val(0) = 0
        b : val(0) = 0
     type = n
   region = sat
reversed = no
      ids = 60.037 uA
     isub = 41.0222 aA
      vgs = 523.447 mV
      vds = 523.447 mV
      vbs = 0 V
      vgb = 523.447 mV
      vdb = 523.447 mV
      vgd = 1.32916 pV
      vth = 502.512 mV
    vdsat = 78.9438 mV
   vfbeff = -1.00379 V
       gm = 1.00019 mS
      gds = 18.5458 uS
     gmbs = 283.567 uS
          ...
```

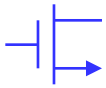
Check operating point and beware of shifts during large transients!



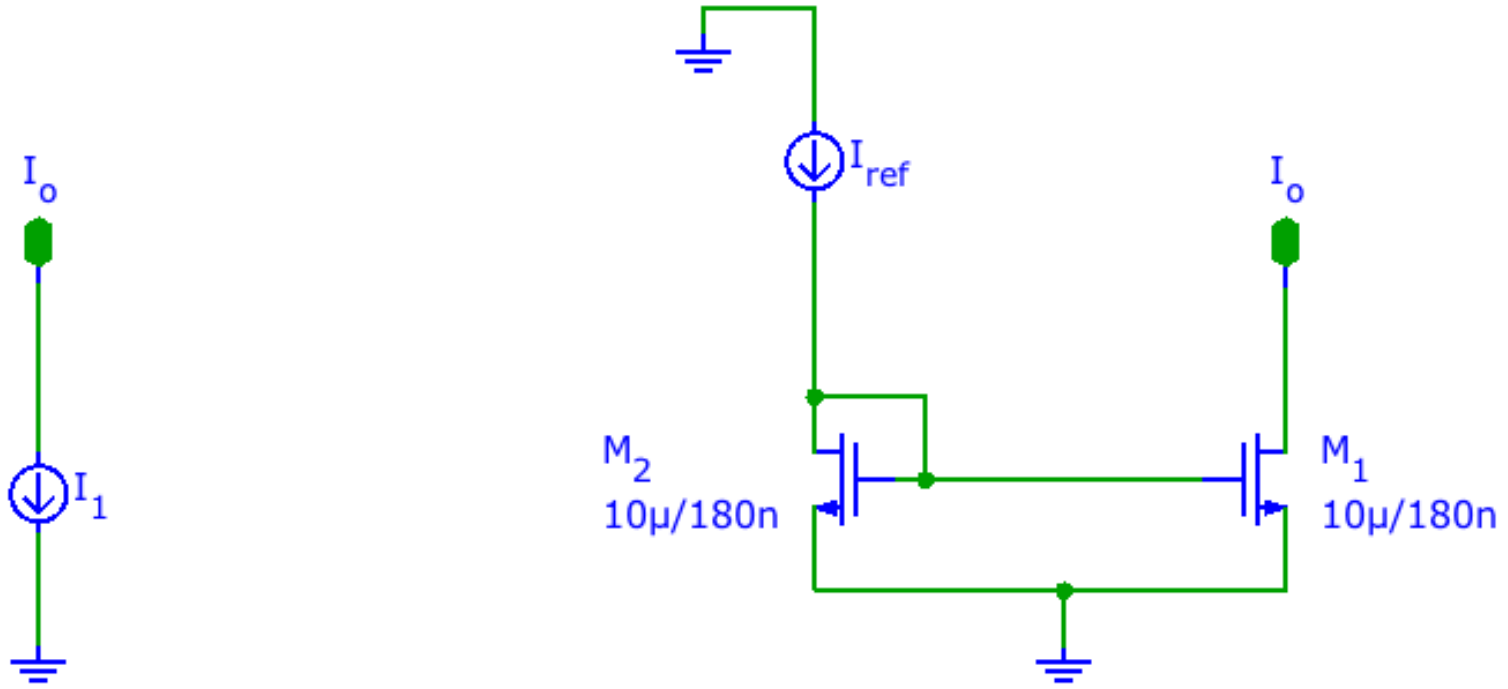
Advanced Analog Integrated Circuits

Current Sources

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

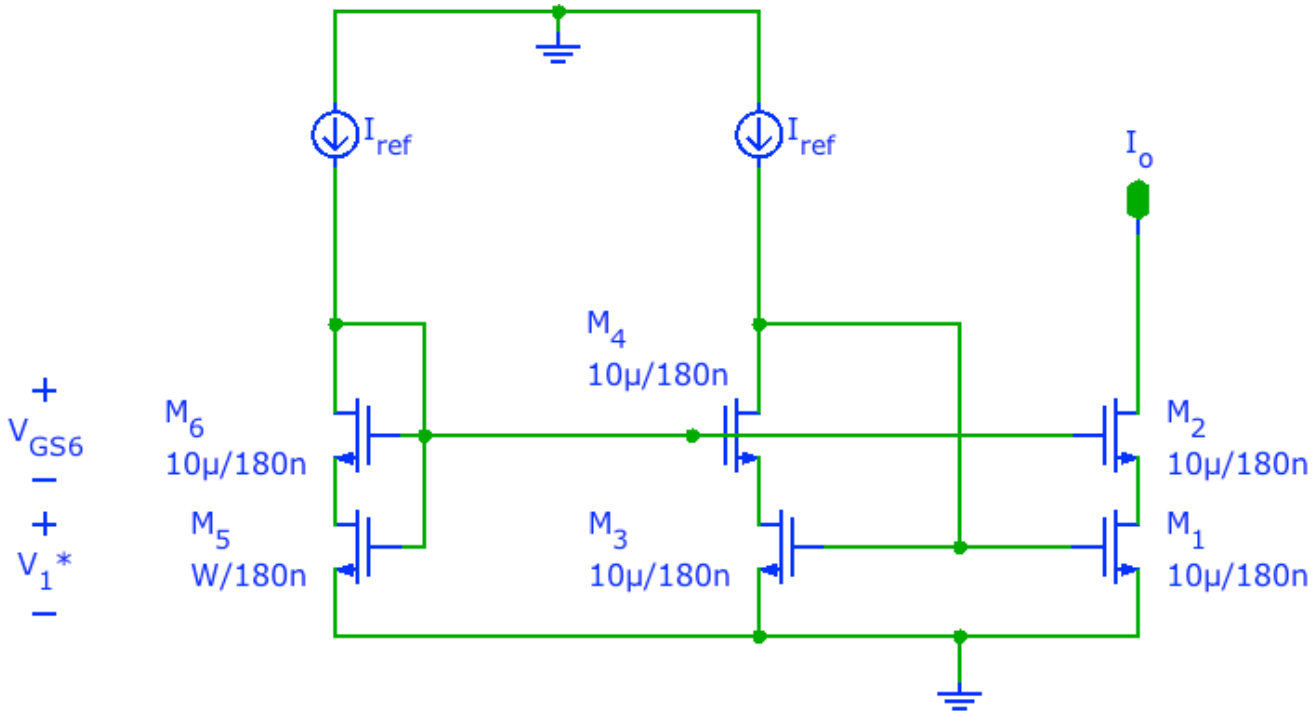


Current Source Realization: Mirror



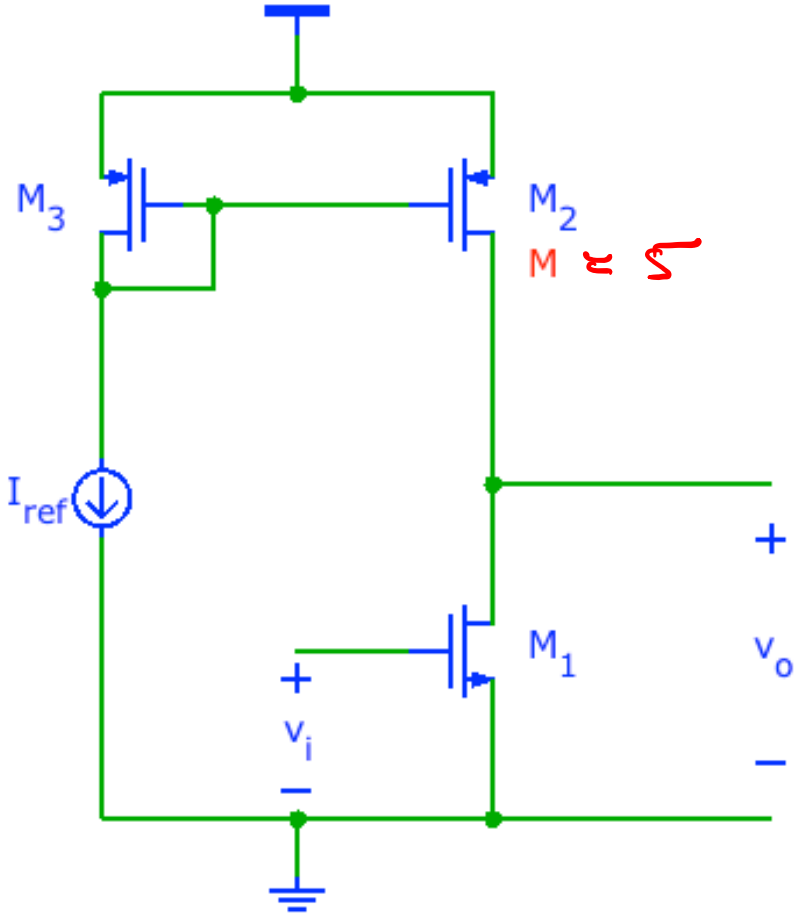
Choices for I_{ref}: resistor, bandgap, constant g_m reference, …

Cascode Bias



- Choose $W_5 \cong {}^{W_1}/_3$ such that $V_{DS1} \cong V_1^* + 50\text{mV}$ (use lookup)
- Note: ok for cascodes to have different W/L
- Insensitive to body-effect

Bias Network Power Dissipation



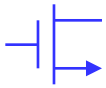
Minimize:

- Share bias network between several amplifiers
- Ratio mirror

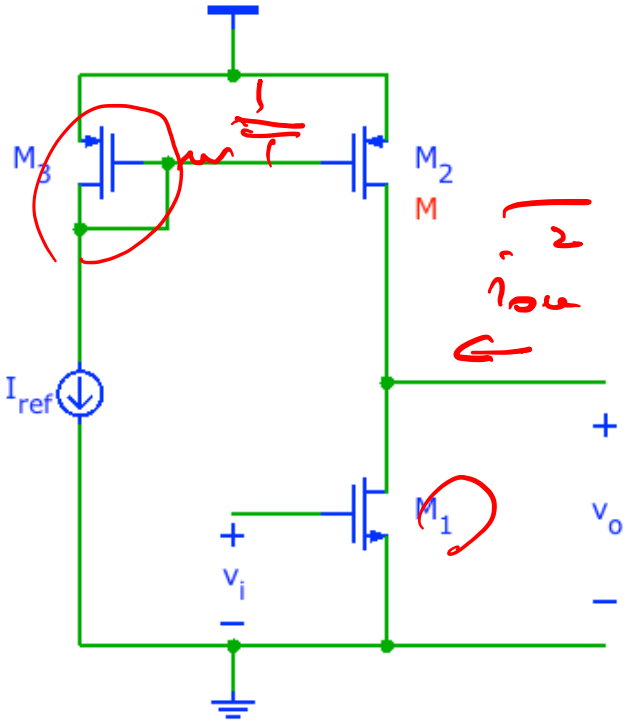
Advanced Analog Integrated Circuits

Noise

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu



Noise



$$\overline{i_{no}^2} = \overline{i_{n1}^2} + \overline{i_{n2}^2} + M^2\,\overline{i_{n3}^2}$$

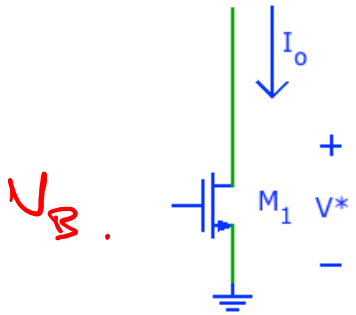
$$= 4kT\gamma g_{m1}\left\{1 + \frac{g_{m2}}{g_{m1}}\cdot(1+M)\right\}\cdot\Delta f$$

$$\alpha = 3$$

$$= 4kT\gamma g_{m1}\left\{1 + \frac{V_1^*}{V_2^*}(1+M)\right\}\Delta f$$

Low Noise Current Source

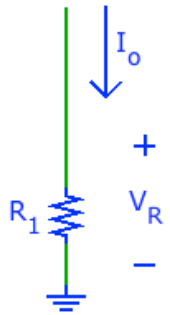
Active (BJT or MOS)



$$R_o = \frac{a_{vo}}{g_m} = \frac{g_m}{2} \cdot \frac{V^*}{I_o}$$

$$\overline{i_{no}^2} = 4kT \cdot \gamma \cdot \frac{I_o}{V^*} \cdot \Delta f$$

Resistor



$$R_o = \frac{V_R}{I_o}$$

$$\overline{i_{no}^2} = 4kT \cdot \frac{I_o}{V_R} \cdot \Delta f$$

Class of Operation

- **Class A ← focus in this course**
  - Constant bias current – runs continuously (e.g. even without signal)
  - (Nominally) constant g_m, pole frequencies
  - Poor power efficiency
- Class B
  - Bias current matches signal amplitude
  - No current when signal amplitude is zero
  - Usually high distortion
- Class AB
  - Class B with (small) quiescent current continuously running
  - Reduced distortion (compared to class B)
  - Used in output stages and buffers
- Class D
  - PWM “digital” output
  - Very high power efficiency
  - E.g. audio amplifiers
- …